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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,626	01/20/2004	Bruce R. Ferguson	MSEMI.113A	8247

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EXAMINER	
BEHM, HARRY RAYMOND	
ART UNIT	**PAPER NUMBER**
2838	

DATE MAILED: 01/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/760,626	FERGUSON, BRUCE R.
	Examiner	Art Unit
	Harry Behm	2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/19/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Paragraph 47 refers to the integrator circuit 210, but Fig. 3 210 and Fig. 5 210 show a low pass filter.

2. Appropriate correction is required.

Claim Objections

3. Claims 1 and 11 are objected to because of the following informalities: Claims 1 and 11 are punctuated with two periods. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being anticipated by Tanaka (US 6,157,182) in view of Shimamori (US 6,204,650) and Farrenkopf (US 6,229,293).

6. With respect to Claim 1, Tanaka discloses a power converter comprising: a load sensor configured to monitor the output (Fig. 3 12) of the peak current detector to change operating modes (Fig. 3 14) for the power converter, wherein the power converter changes from a hysteretic mode ("light load mode") to a

continuous switching mode ("heavy load mode") when the number of peak current pulses (para 51 "current supply cycles") in the burst period exceeds a predetermined number (Fig. 8 32); a peak current detector configured (Fig. 3 13) to sense current through the load and to output a peak current pulse (Fig. 3 SECOND SIGNAL) to the pulse width modulator (Fig. 3 14) to turn off the switching transistor when the sensed current exceeds a peak reference level (Tanaka Fig. 5 I_{LP}). Tanaka does not disclose the use of a pulse frequency modulator (PFM) or that the current should be sensed through the switch. Farrenkopf teaches a boost converter (Fig. 1) with a switching transistor (Fig. 1 N1) and further discloses to sense the current through the switching transistor (Fig. 1 Rs). The use of PFM techniques are widely known and taught by a number of sources including Bittner (US 5,568,044) and Shimamori (US 6,163,143). While Shimamori's implementation of the operation unit (Fig. 19 94) is digital, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the operation unit with analog circuitry because mappings between digital and analog circuits are well known in the art and analog implementations are often more economical when a microcomputer is not available. Shimamori teaches a pulse frequency modulator (Fig. 19 91) configured to control the switching transistor, wherein the pulse frequency modulator is enabled during a burst period in which an output (Fig. 19 OUTPUT) of the power converter is less than a predetermined level (Fig. 19 REFERNCE VALUE). It would have been obvious to one of ordinary skill in the art at the time

of the invention to replace the PWM controller of Tanaka with the PFM controller of Shimamori. The motivation to replace the PWM controller with the PFM controller would be to achieve higher efficiency; a PFM mode requires fewer turn-on transitions to maintain a constant output voltage than does a PWM mode of voltage regulation, thus resulting in a lower gate-drive power dissipation for PFM mode; further a PFM mode can be achieved with a much simpler control circuit having fewer components, thus the power dissipation in the control loop of a PFM mode is less than that of the control loop of a PWM mode. It also would have been obvious to one of ordinary skill in the art at the time of the invention to combine the dual-mode converter of Tanaka with the boost converter of Farrenkopf to create the invention claimed by Ferguson, the reason for doing so would be to obtain the benefit of an output voltage higher than the input voltage. Thus, the combined references teach in addition to the above, the use of a peak current detector (Farrenkopf Fig. 1 Rs) configured to sense current through the switching transistor (Farrenkopf Fig. 1 N1) and to output a peak current pulse (Tanaka Fig. 3 SECOND SIGNAL) to the pulse frequency modulator (Shimamori Fig. 19 91,94) to turn off the switching transistor when the sensed current exceeds a peak reference level (Tanaka Fig. 5 I_{LP}).

7. With respect to Claim 2, Tanaka as above discloses the power converter of Claim 1 further comprising: a feedback comparator (Tanaka Fig. 3 12) configured to monitor the output of the power converter; and a filter circuit (Shimamori Fig. 19 95) coupled to an output of the feedback comparator and

configured to generate a variable voltage (Shimamori Fig. 19 93), wherein the variable voltage is used by the peak current detector (Tanaka Fig. 3 14) as the peak reference level (Tanaka Fig. 5 I_{LP}) when the power converter is operating in the continuous switching mode (Tanaka "heavy load mode") and the power converter changes from the continuous switching mode to the hysteretic mode (Tanaka "light load mode") when the variable voltage (Shimamori Fig. 19 93) falls below a predefined threshold (Tanaka para 5 "predetermined reference level").

8. With respect to Claim 3 Tanaka as above discloses the power converter of Claim 1, wherein the peak reference level (Tanaka Fig. 5 I_{LP}) is substantially constant during the hysteretic mode (Tanaka "light load mode").

9. With respect to Claim 4, Tanaka as above discloses the power converter of Claim 1, wherein the load sensor is a counter (Tanaka Fig. 14 52) that increments with each peak current pulse (Tanaka para 51 "current supply cycles") and resets (Tanaka Fig. 14 54) at the end of each burst period.

10. With respect to Claim 5, Tanaka discloses the power converter of Claim 2, wherein the variable voltage (Shimamori Fig. 19 91) is proportional to the duty cycle of the output of the feedback (Shimamori Fig. 19 Vout). Shimamori does not detail the requirements for the filter. When combined with the feedback comparator of Tanaka (Fig. 3 12), the digital filter would be required to accumulate (integrate) the difference between the reference value and Vout and the filter circuit (Shimamori Fig. 19 95) becomes an integrator and the variable

voltage analog (Shimamori Fig. 19 91) is proportional to the duty cycle of the output of the feedback comparator (Tanaka Fig. 3 12).

11. With respect to Claim 6, Tanaka as above discloses a method to convert operating modes (Tanaka Fig. 3 14) in a switching regulator, the method comprising the steps of: turning on a pulse frequency modulator (Shimamori Fig.19 91,94) for a burst period when an output of the switching regulator is less than a first level (Tanaka Fig. 3 12), wherein one or more switching cycles for a switch occur in the burst period; turning on the switch in each switching cycle until the switch conducts a peak current (Tanaka Fig. 5 I_{LP}) followed by a switch off-time of a predetermined duration (Shimamori Fig. 19 92); and converting from a hysteretic mode (Tanaka "light load mode") to a continuous mode (Tanaka "heavy load mode") when the number of switching cycles (Tanaka para 51 "current supply cycles") in a burst period exceeds a predetermined value (Tanaka Fig.3 32).

12. With respect to Claim 7, Tanaka as above discloses the method of Claim 6 further comprising the steps of: generating a variable threshold (Shimamori Fig. 19 93) to control the peak current conducted by the switch during the continuous mode (Tanaka "heavy load mode"); and converting from the continuous mode to the hysteretic mode (Tanaka "light load mode") when the variable threshold is less than a predefined level (Tanaka Fig. 14 52).

13. With respect to Claim 8, Tanaka as above discloses the method of Claim 6, wherein the peak current is substantially constant (Tanaka Fig. 5 I_{LP}) during the hysteretic mode (Tanaka Fig. 5 I_{LP}).

14. With respect to Claim 9, Tanaka as above discloses the method of Claim 7, wherein the variable threshold (Tanaka Fig. 5 I_{LP}) is generated from a feedback voltage (Shimamori Fig. 19 Vout) indicative of the output of the switching regulator (Shimamori Fig. 19 OUTPUT).

15. With respect to Claim 10, Tanaka as above discloses the method of Claim 6, wherein the switching regulator is a boost converter (Farrenkopf Fig. 1).

16. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being anticipated by Muratov (US 6433525) in view of Shimamori (US 6204650).

17. With respect to Claim 11, Muratov discloses a switching regulator using a dual-mode pulse width modulation technique (Fig. 4 100) comprising: means for sensing a transition from relatively light load current to relatively heavy load current by monitoring switching cycles of a switch (Fig. 4 50 "a counter in the mode switch 50 counts the number of pulses of the new polarity and after n pulses in a row, the mode switches"); and means for operating the switching regulator in a hysteretic mode (Fig. 4 HYSTERETIC CONTROLLER) during relatively light load current, wherein the switch conducts a substantially fixed peak current during the hysteretic mode; and means for operating the switching regulator in a continuous switching mode (Fig. 4 PWM CONTROLLER) during relatively heavy load current, wherein the switch conducts a variable peak current

during the continuous switching mode. Muratov does not disclose the use of pulse frequency modulation (PFM) as the other mode of operation. The use of PFM techniques are widely known and taught by a number of sources including Bittner (US 5,568,044) and Shimamori (US 6,163,143). Shimamori teaches the use of a suitable PFM technique. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the PWM controller of Muratov with the PFM controller of Shimamori to create the invention claimed by Ferguson. The motivation to replace the PWM controller with the PFM controller would be to achieve higher efficiency; a PFM mode requires fewer turn-on transitions to maintain a constant output voltage than does a PWM mode of voltage regulation, thus resulting in a lower gate-drive power dissipation for PFM mode; further a PFM mode can be achieved with a much simpler control circuit having fewer components, thus the power dissipation in the control loop of a PFM mode is less than that of the control loop of a PWM mode.

18. With respect to Claim 12, Muratov in view of Shimamori discloses the switching regulator of Claim 11, further comprising: means for sensing an output of the switching regulator (Fig. 4 20), means for generating a feedback voltage by comparing the sensed output to a reference voltage (Fig. 4 Vo FEEDBACK); and means for controlling the variable peak current based on the feedback voltage (Shimamori Fig. 19 91).

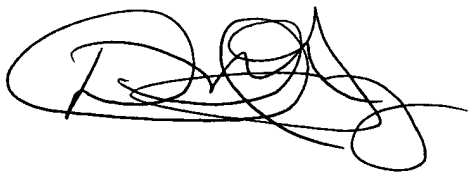
Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bowman (US 6,791,283) discloses a boost converter with current feedback driving a load of LED's.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Behm whose telephone number is 571-272-8929. The examiner can normally be reached on business hours EST.

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Gray can be reached on 571-272-2119. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David Gray
Primary Examiner

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